REMARKS

The present Further Amendment After Final Rejection is being filed in further response to the Office Action of June 9, 2008, and in view of an Advisory Action that was issued after an original Amendment After Final Rejection was filed on September 9, 2008. An RCE is being filed concurrently to permit further prosecution.

Revisions to the claims:

The present Amendment cancels two dependent claims and revises both independent claims. The claims now recite that N type ions and P type ions are implanted into regions of a polysilicon layer, and that the gate electrodes have areas that are smaller than the areas of the doped regions from which they are etched. Although this is not explicitly stated in the specification of this application, an ordinarily skilled person would understand from Figures 3(a) through 3(c) of the application that this is true. Since gate electrodes are formed by etching away some of the N type region and the P type region, the gate electrodes are clearly smaller in size than the regions from which they were formed.

The Amendment also makes other revisions in the claims, including revising independent claim 15 to recite that the etching process is "a multi-stage" process.

The Objections to the Drawings and Specification:

It is not clear from the Advisory Action whether the objections imposed in sections 2 and 4 of the Office Action dated June 9, 2008 were overcome by the arguments against these rejections that were presented in the original Amendment After Final Rejection. As a precautionary measure, to ensure that the present Further Amendment After Final Rejection is fully responsive to the Office Action of June 9, 2008, the arguments are repeated below.

Section 2 of the Office Action objects to the drawings on the ground that Figure 3(c) shows no indication that the polysilicon arrangement is etched, and section 4 objects to changes in the specification regarding Figure 3(c). Section 4 comments, "Specifically, there is nothing in the original disclosure which supports there being a structure remaining in the non-doped polysilicon region after the described etching process." For the reasons

discussed below, the objections in both sections 2 and 4 of the Office Action are respectfully traversed.

The present application discloses that P-type polysilicon and N-type polysilicon etch at different rates (see, for example, the paragraph bridging pages 2 and 3 of the application and the paragraph bridging pages 7 and 8). The application also discloses that non-doped polysilicon etches at a rate which lies between the etching rate of P-type polysilicon and N-type polysilicon (see the paragraph at page 7 of the application, lines 14-25). Since both a P-type polysilicon gate electrode and an N-type polysilicon gate electrode are shown in the original version of Figure 3(c), what the application calls a "dummy gate" of non-doped polysilicon should be present in Figure 3(c).

Furthermore, Figure 3(a) shows implantation of N-type impurities into a region 4 through an opening in resist 3. Figure 3(b) shows implantation of P-type impurities in a region 5 through an opening in a resist layer; the region 6 is not implanted with impurities. The drawings do not show a mask with patterns for etching the N-type and P-type gate electrodes that are shown in Figure 3(c), but an ordinarily skilled person would have understood that a mask is used to permit etching of these gate electrodes. The application advises that dummy gate patterns are disposed on the mask (see page 7, lines 3-7). An ordinarily skilled person would have realized that the result would be a dummy gate electrode in Figure 3(c) as in the replacement drawing sheet that was forwarded with the Amendment filed on March 24, 2008.

Dependent claims 20 and 21:

Section 5 of the Office Action objects to claim 21, and section 6 rejects claims 20 and 21 for new matter. The present Amendment cancels these claims, so the objection and rejection are now moot.

The Rejections on the Prior Art:

Section 7 of the Office Action rejects independent claim 15 (and several dependent claims) for obviousness based on Liau et al (hereafter simply "Liau") and Gabriel et al (hereafter simply "Gabriel), with evidence provided by Lu. Section 8 of the Office Action rejects independent claim 3 (along with various dependent claims) for obviousness based on Liau, Gabriel, and Lee et al (hereafter simply "Lee"), with evidence again being

provided by Lu. For the reasons discussed below, however, it is respectfully submitted that the inventions now defined by independent claims are patentable over these references.

Claim 15, as currently formulated, reads as follows (with emphasis added):

15. A dry etching method for a semiconductor device, comprising:

providing a polysilicon layer formed on a semiconductor substrate;

implanting a first region of the polysilicon layer with N type ions **and a second region** of the polysilicon layer with P type ions, a further region of the polysilicon layer being left as **a non-doped region**; and

simultaneously etching an N type polysilicon gate electrode from the first region, **a P type polysilicon gate electrode** from the second region, and **a non-doped polysilicon dummy gate arrangement** from the non-doped region of the polysilicon layer during **a multi-stage etching process,**

wherein the **N type polysilicon gate electrode has an area that is smaller than the area of the first region of the polysilicon layer** and the **P type polysilicon gate electrode has an area that is smaller than the area of the second region of the polysilicon layer,**

wherein the **non-doped polysilicon dummy gate arrangement has an area that is larger than the total area** occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode, and

wherein the etching process includes at least one etching stage in which **end point detection is based on the etching of the non-doped polysilicon dummy gate arrangement.**

The Liau reference discloses an integrated circuit (which may be CMOS circuit) having an ESD protection transistor with an undoped polysilicon gate. On page 6, the Office Action acknowledges that Liau does not disclose the gate electrodes and undoped polysilicon arrangement being simultaneously etched, where the etching process includes at least one etching stage in which end point detection is based on the etching of the non-doped polysilicon arrangement. For this, the Office Action turns to the Gabriel reference, and draws attention to passages at columns 6 and 7 of the reference and to Figure 5A.

It is respectfully submitted that Gabriel does <u>not</u> teach simultaneously etching an N-type gate electrode, a P-type gate electrode, and an undoped dummy electrode during an etching process where end point detection of one of the etching stages is based on etching of the non-doped dummy gate arrangement. The purpose of the Gabriel reference is to obtain an improvement end point signal during etching. Gabriel achieves this goal by (as explained in the passage at column 3 of the reference, lines 7-14) by

> ...maximizing the use of a faster etching dopant material and minimizing the use of a slower etching dopant material in the gate electrode layer. The faster etching dopant material will etch away faster, and because the gate electrode layer is predominantly made up of the faster etching dopant material, a strong and detectable endpoint signal will be induced when the etchant reaches the silicon dioxide layer.

The passage at column 6 of the reference, lines 41-62, explains that resist 370 in Figure 5A is disposed over a doped portion 540, with no allowance being made for misalignment. The gate etch will "see" only unimplanted polysilicon in portions 560a and 560b, so a strong and consistent endpoint signal can be detected. Because the gate 550 is entirely etched by the time this endpoint signal is generated, it is unnecessary to have another etching stage (see, in particular, the sentence at column 6, lines 59-61).

The paragraph bridging columns 6 and 7 of the Gabriel reference (which includes a passage, heavily relied on by the Office Action, at lines 6-9 of column 7) explains that Figure 5A shows the formation of only one gate electrode, but the same technique can be used to form more than one N-type gate electrodes or P-type gate electrodes, and the gate etch will still see only unimplanted silicon and therefore a strong and consistent endpoint signal can be detected.

In view of the above discussion, it is respectfully submitted that Liau's Figure 5A and the corresponding written disclosure of the reference would not have led an ordinarily skilled person to modify Liau so as to achieve the invention defined by claim 15. Claim 15 now recites "a multi-stage etching process," and Gabriel needs only one etching stage because of the accurate alignment of his mask with respect to the doped region of the polysilicon layer beneath it. The etchant removes all of the non-doped polysilicon at approximately the same time, and this is what causes the strong endpoint signal that Gabriel seeks.

Claim 15 now also provides that a first region of the polysilicon layer is doped with N type ions and a second region is doped with P type ions, and that "the N type polysilicon gate electrode has an area that is smaller than the area of the first region of the polysilicon layer and the P type polysilicon gate electrode has an area that is smaller than the area of the second region of the polysilicon layer." In contrast, the technique shown in Gabriel's Figure 5A (and also in Figure 5B) requires the doped region and the resulting gate electrode to have the same area.

On page 6, the Office Action also acknowledges that Liau does not disclose that the non-doped polysilicon arrangement occupies an area larger than the total area occupied by the N-type polysilicon gate electrode and the P-type polysilicon gate electrode. On page 7, though, the Office Action takes the position that Lu teaches that the gate width of the transistor is proportional to its current-carrying capacity, so gate width should be considered to a result effective variable, where the result is modification of the current carrying capacity. The Office Action continues by asserting that the size of the undoped portion therefore merely constitutes an optimization of ranges. Applicants respectfully disagree.

Claim 15 refers to area, which is a function not only of width, but also of length. If an ordinarily skilled person sought to modify the length of Liau's non-doped gate electrode 40, and in attempt to achieve some desired current-carrying capacity for Liau's ESD transistor, there is no reason to suspect that the result would be a gate occupying an area that is larger than the total area occupied by the two gates 41 in Liau's Figure 7. Furthermore, there is no reason to think that an ordinarily skilled person who wanted to improve Liau's arrangement in some way would have thought it necessary to optimize the current-carrying capacity of Liau's ESD transistor in the first place. The ordinarily skilled person would know that the purpose of an ESD protection transistor is to protect circuitry from a momentarily voltage spike, which would not last long enough for the current through the ESD protection transistor to cause appreciable heating. The ordinarily skilled person would be concerned about voltage, not current, and would therefore have no reason to optimize the current-carrying capacity of an ESD protection transistor.

Claim 15 also recites "simultaneously etching ... a non-doped polysilicon dummy gate arrangement from the non-doped region of the polysilicon layer ...". Gabriel does not etch a dummy gate arrangement from a non-doped region of a polysilicon layer. Instead, the technique shown in Figure 5A of the reference etches all of the non-doped polysilicon away.

Accordingly, it is respectfully submitted that the invention defined by claim 15 is patentable over Liau, Gabriel, and Lu. Independent claim 3 includes limitations similar to those discussed above with respect to claim 15, and the Lee reference does not make up for the shortcomings of Liau and Gabriel. It is respectfully submitted that the invention

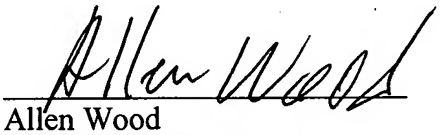
defined by claim 3 would not have been obvious from the prior art, for reasons along the lines discussed above with respect to claim 15.

The remaining claims depend from claim 3 or claim 15 claims and recite additional limitations to further define the invention. They are therefore automatically patentable along with their independent claims and need not be further discussed.

Conclusion:

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



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